PROCESSING HIGH-SPEED DIGITAL SIGNALS

[ABSTRACT OF THE DISCLOSURE]

A first transparent latch (22) receives a first synchronised signal (S1) which changes its logic state synchronously with respect to a clock signal (CLK). A second transparent latch (24) receives a second synchronised signal (S2) output by the first latch (22). When the clock signal has a first logic state (H) the first latch (22) has a non-responsive state and the second latch has a responsive state, and when the clock signal has a second logic state (L) the first latch has the responsive state and the second latch has the non-responsive state.

In such circuitry the change in logic state of a third synchronised signal (S3) output by the second latch (24) is guaranteed to occur in a particular half-cycle of the clock signal, irrespective of process/voltage/temperature (PVT) variations of the circuitry.

Other embodiments relate to clock recovery circuitry having N(≥2) rising-edge and falling-edge latches (Fig. 6); circulating control pattern verification circuitry (Fig. 12); data synchronising circuitry for converting parallel data clocked by a first clock signal into serial data clocked by a second clock signal asynchronous with the first clock signal (Fig. 15); and data recovery circuitry for producing an offset clock signal which can be chosen freely to suit a data eye shape of a received serial data stream (Fig. 21).

[Fig. 3]